CLAIMS

1. An address decoder for selectively applying to word lines of a memory array signals of variable polarity, negative or positive, each signal having a value that varies according to a word line address applied to the decoder, the address decoder comprising:

a group decoder delivering group selection signals of variable polarity for selecting a group of word lines from a plurality of groups of word lines;

at least one subgroup decoder delivering subgroup selection signals of variable polarity for selecting a subgroup of word lines from a plurality of subgroups of word lines, each subgroup of word lines comprising a set of word lines belonging to different groups of word lines; and

word line drivers with one word line driver per word line, each comprising means for multiplexing the group and subgroup selection signals, for selecting and selectively applying one of these signals to a word line.

2. The decoder according to claim 1 wherein:

each group of word lines comprises a respective set of word lines having address bits of identical determined significance; and

each subgroup of word lines comprises a respective set of word lines having address bits of identical determined significance, while belonging to different groups of word lines.

3. The decoder according to claim 2 wherein each group of word lines comprises a set of word lines having identical most significant address bits, and each subgroup of word lines comprises a set of word lines having identical least significant address bits.

4. The decoder according to claim 1 wherein each word line driver comprises MOS-type switch transistors which are both driven on their gate and biased on their drain and their source by the group and subgroup selection signals, and are arranged for selecting one of these signals and for applying it to a word line.

5. The decoder according to claim 4 wherein each word line driver comprises switch transistors each having:

a terminal linked to a word line;

a terminal receiving one of the group or subgroup selection signals; and

a gate receiving another of the group or subgroup selection signals.

6. The decoder according to claim 1 wherein the subgroup decoder comprises:

a first subgroup decoder, delivering first subgroup selection signals having values that vary according to the word line address applied to the address decoder during a phase of erasing memory cells, and is independent of the address applied to the address decoder during phases of reading or programming memory cells; and

a second subgroup decoder delivering second subgroup selection signals having values that vary according to the word line address applied to the address decoder during the phases of reading or programming, and is independent of the address applied to the address decoder during the phase of erasing.

7. The decoder according to claim 6 wherein each of the subgroup decoders receives a first and a second reference voltage and supplies, in addition to a subgroup selection signal, a complementary subgroup selection signal equal to the second reference voltage when the subgroup selection signal is equal to the first reference voltage and equal to the first reference voltage when the subgroup selection signal is equal to the second reference voltage.

8. The decoder according to claim 7 wherein each word line driver comprises:

first MOS transistors having gates that are driven by one of the complementary signals; and

second MOS transistors having gates that are driven by group selection signals.

9. The decoder according to claim 7 wherein each word line driver comprises:

a first MOS transistor having a drain or source terminal linked to a word line, receiving a group selection signal at its gate and receiving a first subgroup selection signal at a source or drain terminal;

a second MOS transistor having a drain or source terminal linked to the word line, receiving the group selection signal at its gate and receiving a second subgroup selection signal at a source or drain terminal;

a third MOS transistor having a drain or source terminal linked to the word line, receiving a first complementary subgroup selection signal at its gate and receiving a second subgroup selection signal at a source or drain terminal; and

a fourth MOS transistor having a drain or source terminal linked to the word line, receiving a second complementary subgroup selection signal at its gate and receiving a first subgroup selection signal at a source or drain terminal.

10. The decoder according to claim 1 wherein the group and subgroup decoders receive two reference voltages that are respectively equal to a non-read voltage and a read voltage during reading of memory cells of the memory array.

11. The decoder according to claim 1 wherein the group and subgroup decoders receive two reference voltages that are respectively equal to a programming

inhibit voltage and a programming voltage during programming of memory cells of the memory array.

12. The decoder according to claim 1 wherein the group and subgroup decoders receive two reference voltages that are respectively equal to an erase voltage and to an erase inhibit voltage during erasing of memory cells of the memory array.

13. The decoder according to claim 1 wherein:

the group and subgroup decoders receive two reference voltages that are respectively equal to a non-read voltage and a read voltage during reading of memory cells of the memory array;

the group and subgroup decoders receive two reference voltages that are respectively equal to a programming inhibit voltage and a programming voltage during programming of the memory cells;

the group and subgroup decoders receive two reference voltages that are respectively equal to an erase voltage and to an erase inhibit voltage during erasing of the memory cells; and

the programming voltage is positive, the programming inhibit voltage and the erase voltage are negative, the non-read and erase inhibit voltages are zero.

14. The decoder according to claim 1 comprising a predecode stage supplying predecoding signals to the group and subgroup decoders.

15. The decoder according to claim 1 wherein the group decoder and the subgroup decoder supply positive, negative, and zero selection signals.

16. The decoder according to claim 1 wherein the group decoder comprises voltage elevator circuits for transforming a logic signal equal to 1, having a

determined positive level of voltage, into a logic signal having a higher positive level of voltage, equal to a reference voltage supplied to the voltage elevator circuits.

17. The decoder according to claim 1 wherein the group and subgroup decoders comprise voltage selector switches for transforming logic signals on 0 and on 1 into signals having different negative levels of voltage.

18. The decoder according to claim 1 wherein the group and subgroup decoders comprise voltage selector switches arranged for transforming a logic signal on 0 into a negative voltage signal and a logic signal on 1 into a positive voltage signal.

19. A memory device, comprising:

a memory array having memory elements arranged in a plurality of rows that are controlled by a corresponding plurality of word lines; and

an address decoder for selectively applying to the word lines of the memory array signals that are negative during a first phase and positive during a second phase, each signal having a value that varies according to a word line address applied to the decoder, the address decoder comprising:

a group decoder delivering negative and positive group selection signals for selecting a group of the word lines from a plurality of groups of the word lines;

a first subgroup decoder delivering negative and positive subgroup selection signals for selecting a subgroup of the word lines from a plurality of subgroups of the word lines, each of the subgroups of word lines comprising a set of word lines belonging to different groups of word lines; and

a plurality of word line drivers connected to the plurality of word lines, respectively, such that each word line driver corresponds to a respective one of the word lines, each word line driver being structured to drive the corresponding word lines based on the group and subgroup selection signals.

20. The memory device of claim 19 wherein:

each group of word lines comprises a respective set of word lines having address bits of identical determined significance; and

each subgroup of word lines comprises a respective set of word lines having address bits of identical determined significance, while belonging to different groups of word lines.

21. The memory device of claim 19 wherein each word line driver comprises MOS-type switch transistors having respective gates driven by one of the group selection signals, respective first conduction terminals bias by respective subgroup selection signals, and respective second conduction terminals connected to each other and to the corresponding word line.

22. The memory device of claim 19 wherein the subgroup decoder comprises:

a first subgroup decoder connected to first and second reference voltages and structured to provide a first subgroup selection signal equal to one of the first and second reference voltages and a complementary first subgroup selection signal that is a complement of the first subgroup selection signal; and

a second subgroup decoder connected to the first and second reference voltages and structured to provide a first subgroup selection signal equal to one of the first and second reference voltages and a complementary first subgroup selection signal that is a complement of the first subgroup selection signal, wherein each word line driver includes:

a first MOS transistor having a gate connected to the group decoder, a first conduction terminal connected to receive the first subgroup selection signal from the first subgroup decoder, and a second conduction terminal connected to the corresponding word line;

a second MOS transistor having a gate connected to the group decoder, a first conduction terminal connected to receive the second subgroup selection signal from the second subgroup decoder, and a second conduction terminal connected to the corresponding word line;

a third MOS transistor having a gate connected to receive the complementary second subgroup selection signal from the second subgroup decoder, a first conduction terminal connected to receive the first subgroup selection signal from the first subgroup decoder, and a second conduction terminal connected to the corresponding word line; and

a fourth MOS transistor having a gate connected to receive the complementary first subgroup selection signal from the first subgroup decoder, a first conduction terminal connected to receive the second subgroup selection signal from the first subgroup decoder, and a second conduction terminal connected to the corresponding word line.

23. The memory device of claim 19 wherein the group decoder and the subgroup decoder supply positive, negative, and zero selection signals.

24. The memory device of claim 19 wherein the group decoder comprises a voltage elevator circuit for transforming a logic signal equal to 1, having a determined positive level of voltage, into a logic signal having a higher positive level of voltage, equal to a reference voltage supplied to the voltage elevator circuit.

25. The memory device of claim 19 wherein the group and subgroup decoders comprise voltage selector switches for transforming logic signals 0 and 1 into signals having different negative levels of voltage.

26. The memory device of claim 19 wherein the group and subgroup decoders comprise voltage selector switches arranged for transforming a logic signal 0 into a negative voltage signal and a logic signal 1 into a positive voltage signal.

27. A line decoder for selectively applying to a line of a memory array signals of variable polarity, negative or positive, the decoder comprising:

a first MOS transistor having a gate connected to receive a control signal, a first conduction terminal connected to receive a first selection voltage, and a second conduction terminal connected to the line of the memory array;

a second MOS transistor having a gate connected to the gate of the first MOS transistor, a first conduction terminal connected to receive a second selection voltage, and a second conduction terminal connected to the line of the memory array;

a third MOS transistor having a gate connected to receive a complementary second selection voltage that is complementary to the second selection voltage, a first conduction terminal connected to first conduction terminal of the first MOS transistor, and a second conduction terminal connected to the line of the memory array; and

a fourth MOS transistor having a gate connected to receive a complementary first selection voltage that is complementary to the first selection voltage, a first conduction terminal connected to the first conduction terminal of the second MOS transistor, and a second conduction terminal connected to the line of the memory array.

28. A method of selectively applying to word lines of a memory array signals of variable polarity, negative or positive, each signal having a value that varies according to a word line address, the method comprising:

delivering group selection signals of variable polarity for selecting a group of word lines from a plurality of groups of word lines;

delivering subgroup selection signals of variable polarity for selecting a subgroup of word lines from a plurality of subgroups of word lines, one of the subgroups of word lines comprising a set of word lines belonging to different groups of word lines; and

multiplexing the group and subgroup selection signals to select and selectively apply one of these signals to one of the word lines.